

**Recognition Of VLSI Module Isomorphism By
Emmanouil N. Zagourakis**

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Graphs Introduction Isomorphism artificial intelligence technique used by many applications in pattern recognition VLSI Physical Design

Orthogonal drawings of graphs for the automation

This article shows the recent developments on orthogonal drawings of graphs which have applications for the automation of VLSI Isomorphism of planar graphs

Recognition of vlsi module isomorphism

Recognition of VLSI module isomorphism Zagourakis, Emmanouil N. Name: 90Mar_Zagourakis.pdf. Size: 4.193Mb. Format: PDF. View/ Open.

Rasterization theory, architectures, and

This paper first presents a theory for rasterizing the class of two-dimensional problems isomorphism relationship class of two-dimensional problems: VLSI

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ADA230298. Title : Recognition of VLSI Module Isomorphism. Descriptive Note : Master's thesis, Corporate Author : NAVAL POSTGRADUATE SCHOOL MONTEREY CA

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The purpose of this study is to determine whether or not a program could be developed to examine isomorphism between parts of a VLSI layout. Many simulation files

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information embedded in a pictorial graph and can be used to build the knowledge base for the representation and recognition VLSI implementation of a

Computer vision applications with the associative

The ASP (Associative String Processor) (i.e., VLSI, WSI, The matrix M_k^+ , is tested for isomorphism

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Exploiting binary translation for fast asip design

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..... 2.2.1 2.2.2 2.2.3 2.2.4 2.2.5 2.2.6 2.3 Graph Isomorphism each module of the hardware has to

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a program could be developed to examine isomorphism between parts of a VLSI that recognition of elements in a Zagourakis, Emmanouil N. PDF Url

Placement of circuit modules using a graph space

"A Method for Determining the Isomorphism of Graphs," Master demands of very large scale integration for VLSI module generation that uses

Determination of macromolecular structures from

Determination of macromolecular structures from anomalous diffraction isomorphism and positively charged groove that might be the recognition

Patent us7243317 - parameter checking method for

Parameter checking method for on-chip ESD protection circuit physical design layout recognition using subgraph isomorphism, reduction module

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